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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,136	07/14/2003	David Mark	X-1269-1P US	6066

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EXAMINER	
HOLLINGTON, JERMELE M	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 11/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,136	MARK ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-18 and 20-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15 and 16* is/are allowed.

6)☒ Claim(s) *1, 3-14, 17-18 and 20-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Note to applicant that Jimmy Nguyen is no longer prosecuting this case. Ex. Jermele Hollington is now prosecuting this case.

Response to Arguments

1. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Specification

2. The disclosure is objected to because of the following informalities: in paragraph [0001], the examiner will like to suggest updating the co-pending application.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 3-14, 17-18 and 20-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Whetsel (6717429).

Regarding claims 1 and 17, Whetsel discloses [see Figs. 11A-12A] test configuration comprising: an integrated circuit (die 601) to be tested; an I/0 pad (I/O pad 1103) of the integrated circuit (601); an output buffer (output buffer 907), wherein an output terminal (see

11B) of the output buffer (907) is coupled to the I/0 pad (1103); a current injector (combination of I/O control 1111, test enable 609 and AND gate 901) on the integrated circuit (601) coupled to the I/0 pad (1103) for injecting a current at the I/0 pad (1103); and a detector (compare circuit 908) on the integrated circuit (601) coupled to the I/0 pad (1103) for detecting a logic level of the I/0 pad (1103).

Regarding claim 3, Whetsel discloses the output buffer (907) is a tri-state buffer [see col. 11, line 54].

Regarding claim 4, Whetsel discloses an input buffer (input buffer 1115), wherein an input terminal [see Fig. 11B] of the input buffer (1115) is coupled to the I/O pad (1103).

Regarding claim 5, Whetsel discloses the current injector (1111, 609, and 901) is selectively enabled by a memory bit.

Regarding claim 6, Whetsel discloses the current injector (609 and 901) is a resistive element on the integrated circuit (601) coupled between the I/O pad (1103) and a voltage reference node (input pad 602).

Regarding claim 7, Whetsel discloses the resistive element (901) is a transistor.

Regarding claim 8, Whetsel discloses a gate of the transistor (901) is coupled to a memory bit (memory 704).

Regarding claims 9-10, Whetsel discloses the voltage reference node is a power node or a ground node.

Regarding claim 11, Whetsel discloses the integrated circuit (601) is one of a plurality of integrated circuits on a wafer (see Fig. 14).

Regarding claim 12, Whetsel discloses the integrated circuit (601) comprises a plurality of I/O pads (1103), the test configuration further comprising [see Fig. 14]: a probe card (probe card 1401) coupled to a subset of the plurality of I/O pads (1103); and automated test equipment (tester 401) coupled to the probe card (1401).

Regarding claim 13, Whetsel disclose the integrated circuit (601) is a programmable logic device.

Regarding claim 14, Whetsel discloses the detector (704 inside 908) is a boundary scan cell.

Regarding claim 18, Whetsel discloses comparing [via compare circuit 908] the detected logic value with an expected value; and if the detected logic value and the expected value do not match, rejecting the integrated circuit (601).

Regarding claim 20, Whetsel discloses the output value is a logic low, further comprising: if the detected logic value is not a logic low, rejecting the integrated circuit (601).

Regarding claim 21, Whetsel discloses the output value is a first output value and wherein the detected logic value is a first detected logic value, further comprising: driving a second output value at the I/O pad (1103) through the output buffer (907), wherein the second output value is a logic high; detecting [via circuit 908] a second logic value of the I/O pad (1103); and if the second detected logic value is not a logic high, rejecting the integrated circuit (601).

Regarding claim 22, Whetsel discloses the step of rejecting the integrated circuit (601) comprises discarding the integrated circuit (601) after the integrated circuit (601) is diced from a wafer.

Regarding claim 23, Whetsel discloses receiving an input value through an input buffer (1115) coupled to the I/O pad (1103).

Regarding claim 24, Whetsel discloses storing the detected logic value in a boundary scan cell (704) of the integrated circuit (601); scanning out the stored logic value [via scan output).

Regarding claim 25, Whetsel discloses receiving the scanned logic value through a probe card (1401); and analyzing the received logic value with automated test equipment (401) at wafer sort.

Regarding claim 26, Whetsel discloses stepping the probe card (1401) over each of a plurality of integrated circuits (601) on a wafer.

Regarding claim 27, Whetsel discloses the logic level detected by the detector (908) indicates whether the output buffer (907) meets a voltage specification of the output buffer (907).

Regarding claim 28, Whetsel discloses determining whether the output buffer (907) passes a gross output buffer voltage test.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO-892 for details.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:00 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jermele M. Hollington
Primary Examiner
Art Unit 2829

JMH
November 7, 2006